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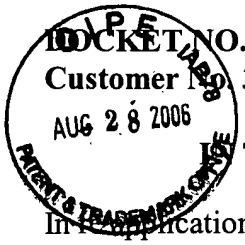

DOCKET NO. 01-B-079 (STMI01-01079) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Srikanth R. Muroor
Serial No.:	10/060,454
Filed:	January 30, 2002
For:	FAST TURN-OFF SLOW TURN-ON ARBITRATOR FOR REDUCING TRI-STATE DRIVER POWER DISSIPATION ON A SHARED BUS
Group No.:	2111
Examiner:	Thomas J. Cleary

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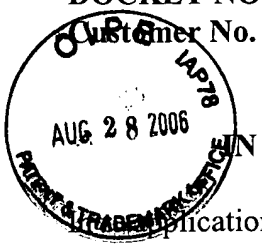
Customer No. 30425



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SUBSTITUTE APPEAL BRIEF

In response to the Notice of Non-Compliant Appeal Brief dated August 15, 2006, the Applicants respectfully submit this Substitute Appeal Brief.

The Appellant has appealed to the Board of Patent Appeals and Interferences from the decision of the Examiner dated January 9, 2006, finally rejecting Claims 1-21. As April 9, 2006, was a Sunday, the Appellant timely filed a Notice of Appeal on April 10, 2006. The Notice of Appeal was received by the U.S. Patent and Trademark Office on April 14, 2006. The Appellant respectfully submits this substitute brief on appeal.

REAL PARTY IN INTEREST

This application is currently owned by STMicroelectronics, Inc. as indicated by an assignment recorded on June 14, 2006 in the Assignment Records of the U.S. Patent and Trademark Office at Reel 012986, Frame 0688.

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this pending appeal.

STATUS OF CLAIMS

Claims 1-21 have been rejected pursuant to a final Office Action dated January 9, 2006. Claims 1-21 are presented for appeal. A copy of all claims is provided in Appendix A.

STATUS OF AMENDMENTS

No amendments were submitted and refused entry after issuance of the final Office Action dated January 9, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER

Regarding Claim 1, a bus arbitrator includes an input circuit, a delay circuit and a comparator circuit. (*Application: Figures 4 and 5*). The input circuit receives first and second bus access request signals from first and second bus devices, respectively. (*Application: Page 2, Lines 8-11*). The input circuit outputs the second bus access request signal when the first bus access request signal is not enabled and blocks the second bus access request signal when the first bus access request signal is enabled. (*Application: 405, 410, Figures 4 and 5; Page 13, Lines 8-10*). The input circuit is associated with a first delay. (*Application: Page 13, Lines 10-13*).

The delay circuit generates time-delayed first and second bus access request signals, associated with a second delay, from the first and second bus access request signals, respectively. (*Application: Page 13, Lines 14-18; Page 13, Line 22, through Page 14, Line 4; Page 15, Lines 5-9*). The comparator circuit generates a first line driver enable signal only if both the first bus access request signal and the time-delayed first bus access request signal are enabled, and generates a second line driver enable signal only if both the second bus access request signal and the time-delayed second bus access request signal are enabled. (*Application: Page 13, Line 14, through Page 14, Line 7; Page 15, Line 10, through Page 16, Line 3*).

The second delay, associated with the delay circuit, delays low-to-high transitions in the first and second line driver enable signals by no more than one-half of a clock cycle of a clock signal. (*Application: Page 13, Lines 5-7*). The first delay, associated with the input circuit, delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but

the input circuit does not delay high-to-low transitions in the first line driver enable signal. (*Application: Page 13, Lines 8-12*).

Regarding Claim 9, a shared bus system includes N bus devices that are capable of requesting access to a shared bus. (*Application: 120A-120C, Figure 1; Page 12, Lines 3-6*). The system also includes M tristate line drivers, each of which has a logic bit input from a bus device and an output to the shared bus. (*Application: 130A-130C, Figure 1; Page 11, Lines 17-20*). Each line driver output either outputs the logic bit on its input or puts its output into a high impedance state, according to whether an associated line driver enable signal is enabled or disabled, respectively. (*Application: Page 11, Lines 17-20*).

The system also includes a bus arbitrator that is operable to activate and de-activate the tristate line drivers. (*Application: 110, Figure 1; Page 12, Lines 6-10*). The bus arbitrator includes an input circuit, a delay circuit and a comparator circuit. (*Application: Figures 4 and 5*). The input circuit receives first and second bus access request signals from first and second ones of the N bus devices, respectively. (*Application: Page 2, Lines 8-11*). The input circuit outputs the second bus access request signal when the first bus access request signal is not enabled and blocks the second bus access request signal when the first bus access request signal is enabled. (*Application: 405, 410, Figures 4 and 5; Page 13, Lines 8-10*). The input circuit is associated with a first delay. (*Application: Page 13, Lines 10-13*).

The delay circuit generates time-delayed first and second bus access request signals, associated with a second delay, from the first and second bus access request signals, respectively. (*Application: Page 13, Lines 14-18; Page 13, Line 22, through Page 14, Line 4; Page 15, Lines 5-9*).

The comparator circuit generates a first line driver enable signal only if both the first bus access request signal and the time-delayed first bus access request signal are enabled, and generates a second line driver enable signal only if both the second bus access request signal and the time-delayed second bus access request signal are enabled. (*Application: Page 13, Line 14, through Page 14, Line 7; Page 15, Line 10, through Page 16, Line 3*).

The second delay, associated with the delay circuit, delays low-to-high transitions in the first and second line driver enable signals by no more than one-half of a clock cycle of a clock signal. (*Application: Page 13, Lines 5-7*). The first delay, associated with the input circuit, delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but the input circuit does not delay high-to-low transitions in the first line driver enable signal. (*Application: Page 13, Lines 8-12*).

Regarding Claim 17, a method is recited for use in a shared bus system that includes N bus devices that are capable of requesting access to a shared bus. The method for activating and deactivating tristate line drivers between the shared bus and the bus devices includes receiving a first bus access request signal from a first bus device and receiving a second bus access request from a second bus device. (*Application: Page 12, Lines 3-8*). The method also includes, associated with a first delay, blocking the second bus access request signal when the first bus access request signal is enabled. (*Application: 405, 410, Figures 4 and 5; Page 13, Lines 8-10*).

The method further includes generating time-delayed first and second bus access request signals, associated with a second delay, from the first and second bus access request signals, respectively. (*Application: Page 13, Lines 14-18; Page 13, Line 22, through Page 14, Line 4;*

Page 15, Lines 5-9). The method also includes comparing the first bus access request signal and the time-delayed first bus access request signal and generating a first line driver enable signal only if both the first bus access request signal and the time-delayed first bus access request signal are enabled. (*Application: Page 13, Line 14, through Page 14, Line 7; Page 15, Line 10, through Page 16, Line 3*).). The method also includes comparing the second bus access request signal and the time-delayed second bus access request signal and generating a second line driver enable signal only if both the second bus access request signal and the time-delayed second bus access request signal are enabled. (*Application: Page 13, Line 14, through Page 14, Line 7; Page 15, Line 10, through Page 16, Line 3*).

The second delay delays low-to-high transitions in the first and second line driver enable signals by no more than one-half of a clock cycle of a clock signal. (*Application: Page 13, Lines 5-7*). The first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but the input circuit does not delay high-to-low transitions in the first line driver enable signal. (*Application: Page 13, Lines 8-12*).

GROUNDS OF REJECTION

1. Claims 1-4, 9-12 and 17-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art ("*AAPA*") in view of U.S. Patent No. 3,886,543 to Marin ("*Marin*").

2. Claims 5-6 and 13-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *AAPA* in view of *Marin* and further in view of U.S. Patent No. 5,306,963 to *Leak*, et al. ("*Leak*").

3. Claims 7-8 and 15-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over *AAPA* in view of *Marin* and further in view of FREDERICK J. HILL & GERALD R. PETERSON, COMPUTER AIDED LOGICAL DESIGN: WITH EMPHASIS ON VLSI § 4.1 (4th ed. 1993) ("*Hill*").

ARGUMENT

I. GROUND OF REJECTION #1

The rejection of Claims 1-4, 9-12 and 17-21 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

A. OVERVIEW

Claims 1-4, 9-12 and 17-21 were rejected under 35 U.S.C. ' 103(a) as being unpatentable over Applicant's Admitted Prior Art ("*AAPA*") in view of U.S. Patent No. 3,886,543 to Marin ("*Marin*").

B. STANDARD

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the Appellant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the Appellant is entitled to grant

of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on Appellant's disclosure. (*MPEP § 2142*).

C. THE APPLICANT'S ADMITTED PRIOR ART

Figure 2 of the specification shows a simple static priority-based arbitration mechanism. First and second bus access request signals are input to a bus arbitrator. The first bus access request signal is passed through an inverter and coupled to one input of an AND gate. The second bus access request signal is coupled to a second input of the AND gate. As a result, the second bus access request signal is blocked when the first bus access request signal is enabled. The first bus access request signal is coupled unmodified to a first tristate line driver and the output of the AND gate is coupled to a second tristate line driver. The first tristate line driver, when enabled, allows a

bus device associated with the first bus access request signal to drive a shared bus. The second tristate line driver, when enabled, allows a bus device associated with the second bus access request signal to drive the shared bus. (*Application: Figure 2; Page 3, Line 10, through Page 4, Line 7*).

D. THE *MARIN* REFERENCE

Marin describes a circuit for debouncing repetitively scanned, manually operable keyswitches. (*Marin, Col. 1, Lines 5-11*). When a keyswitch is depressed, its electrical contacts may bounce open and closed one or more times before settling into a closed position. (*Marin, Col. 1, Lines 26-32*). A keyswitch input signal is coupled to a first shift register cell, whose output is coupled to a second shift register cell. Both shift register cells are coupled to a common clock signal. (*Marin, Col. 4, Lines 10-21*). The keyswitch input signal and the outputs of the two shift register cells are coupled to a three-input AND gate, thereby providing the AND gate with the current state of the keyswitch and its time-delayed samples of its state at the two previous active clock edges. (*Marin, Col. 4, Lines 32-40*). The output of the AND gate goes TRUE only when all three successive samples of the keyswitch state are true. (*Marin, Col. 4, Lines 47-50*).

E. CLAIM 1

Claim 1 recites a bus arbitrator, which includes:

> an input circuit receiving a first bus access request signal from a first bus device and a second bus access request signal from a second bus device, the input circuit outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal

when the first bus access request signal is enabled, the input circuit associated with a first delay;

a delay circuit generating a time-delayed first bus access request signal from the first bus access request signal and a time-delayed second bus access request signal from the second bus access request signal, the delay circuit associated with a second delay; and

a comparator circuit generating a first line driver enable signal only if both the first bus access request signal and the time-delayed first bus access request signal are enabled and generating a second line driver enable signal only if both the second bus access request signal and the time-delayed second bus access request signal are enabled,

wherein the second delay delays low-to-high transitions in the first and second line driver enable signals by no more than one-half of a clock cycle of a clock signal, and wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but does not delay high-to-low transitions in the first line driver enable signal.

The Examiner asserts that *AAPA* teaches a bus arbitrator including an input circuit receiving first and second bus access request signals from first and second bus devices, respectively, with the input circuit outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled. (*01/09/06 Office Action, Section 3, Page 2*). The Examiner further asserts that the AND gate and inverter of the *AAPA* inherently have a first delay and, because the first bus access request signal does not pass through the AND gate and inverter, high-to-low transitions in the first bus access request signal are not delayed by the first delay. (*01/09/06 Office Action, Section 3, Page 2*).

The Examiner acknowledges that the *AAPA* does not teach a delay circuit generating time-delayed first and second bus access request signals, associated with a second delay, from the first and second bus access request signals, respectively, or a comparator circuit generating a first line driver

enable signal only if both the first bus access request signal and the time-delayed first bus access request signal are enabled, and generates a second line driver enable signal only if both the second bus access request signal and the time-delayed second bus access request signal are enabled, wherein the second delay delays low-to-high transitions in the first and second line driver enable signals by no more than one-half of a clock cycle of a clock signal. (*01/09/06 Office Action, Section 3, Pages 2-3*). However, the Examiner asserts that *Marin* describes a delay circuit that receives a signal and generates a time-delayed version of the signal and a comparator circuit that generates an output signal only if both the signal and the time-delayed signal are enabled. (*01/09/06 Office Action, Section 3, Page 3*). The Examiner further asserts that the delay circuit delays low-to-high transitions of the output signal by less than one-half of a clock cycle of a clock signal. (*01/09/06 Office Action, Section 3, Page 3*). The Examiner also argues that, because the first delay of the *AAPA* is simply the propagation delay of a chain of two basic gates, the first delay is inherently shorter than that provided by the delay circuit of *Marin*, which is equal to the time for shifting an input through a shift register. (*01/09/06 Office Action, Section 3, Page 3*).

Finally, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of *AAPA* with the delay and comparator circuits of *Marin* on both the first and second bus access request signals "in order to provide a debounce delay period which ensures that the signal has reached a steady state and thus increases fault tolerance." (*01/09/06 Office Action, Section 3, Page 4*).

The rejection of claim 1 under 35 U.S.C. § 103 is improper and should be withdrawn for four reasons. First, the Examiner has made an unsupported assertion of a claim limitation being found

inherently in the prior art. Second, the *Marin* reference, directed at debounce logic for keyswitches, is non-analogous art to Claim 1, directed to a bus arbitrator. Third, there is no motivation to combine reference teachings. Fourth, no reasonable expectation of success in the combination of the references is found in the prior art.

1. The Examiner has made an unsupported assertion of a claim limitation being inherently taught in the prior art.

The Examiner asserts, without substantiation, that the delay of a signal propagating through an inverter and an AND gate is inherently shorter than that provided by the delay circuit of *Marin*. While the delay circuit of is labeled a shift register cell, the circuit functions as a simple latch or flip-flop, as acknowledged by the Examiner at Section 21, page 12, of the January 9, 2006 Office Action. The Appellant disagrees that the number of gates in a latch or flip-flop is such that the delay through the delay circuit of *Marin* is inherently greater than the delay of a signal propagating through an inverter and an AND gate. Furthermore, there is no teaching in *Marin* of the implementation of its delay circuit to inform the Examiner's assertion that its propagation delay is necessarily greater than that through an inverter and an AND gate.

2. The Marin reference is non-analogous art to the claims of the present application.

The *Marin* reference is directed to debounce logic in a keyboard switch scanner. When a keyswitch is depressed, the contacts may bounce. The *Marin* reference teaches that it is advisable for a switch scanner to combine three successive samples of the keyswitch status to ensure that the

contacts have ceased bouncing. (*Marin, Col. 7, lines 50-56*) In contrast, the claims of the present application are directed to a bus arbitrator for use with circuits that operate on a shared bus driven by buffers having tri-state outputs. The claimed invention eliminates bus contentions by ensuring that the turn-off time of a line driver ceasing to drive the shared bus is shorter than the turn-on time of a line driver beginning to drive the shared bus. *(Application, page 6, first paragraph)*. As such, the *Marin* reference, directed at sensing mechanical switch contact bounce, is not analogous art to the arbitrator for a shared bus system claimed in the present application.

3. There is no motivation to combine the cited references as proposed by the Examiner.

There is no motivation to combine the cited references as proposed by the Examiner. The Examiner's proposed motivation for adding elements of the circuit of *Marin* to the bus arbitrator of the *AAPA* does not address any problem faced by the person of ordinary skill designing a bus arbitrator. A bus access request signal is an output of a semiconductor switch, not a mechanical switch, and, as such, is not subject to contact bounce. Thus, the person of ordinary skill designing a bus arbitrator would have no motivation to "provide a debounce delay period which ensures that the signal has reached a steady state and thus increases fault tolerance" as suggested by the examiner.

Furthermore, the *Marin* reference describes the use of two shift register cells and a three-input AND gate, to combine a current sample of keyswitch contact status with two preceding samples. The circuit signals a switch closure only when three successive samples indicate that the switch is closed. The Examiner asserts, however, that a person of ordinary skill would have found it obvious to modify the bus arbitrator of the prior art with a subset of the circuitry of the *Marin*

reference—only a single shift register cell and a two-input AND gate. The Appellant respectfully submits that the Examiner improperly uses the claims of the present application as a template in selecting portions of the *Marin* reference to combine with the prior art bus arbitrator. Thus, there is no motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine reference teachings as proposed in the Office Action.

4. No reasonable expectation of success in the combination of the references is found in the prior art.

Finally, even were a person of ordinary skill to combine portions of the circuitry of the *Marin* reference with the prior art bus arbitrator, as proposed by the Examiner, no reasonable expectation of success in such a combination may be found in the prior art. While *Marin* describes the benefit of using two shift register cells and a three-input AND gate, it teaches no benefit in using a single shift register cell and a two-input AND gate. As such, the expectation of success in the combination of cited references is found not in the prior art, but in the Applicant's disclosure.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 1. Accordingly, the Appellant respectfully requests that the final rejection of Claim 1 be withdrawn and that Claim 1 be passed to allowance.

F. CLAIM 2

Claim 2 recites the bus arbitrator of Claim 1, wherein the comparator circuit disables the first line driver enable signal if either of the first bus access request signal or the time-delayed first bus access request signal is disabled, and disables the second line driver enable signal if either of the second bus access request signal or the time-delayed second bus access request signal is disabled.

As claim 2 depends from claim 1, the arguments above with regard to claim 1 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA* or *Marin* teaches a comparator circuit disabling a first or second line driver enable signal if either of a first or second bus access request signal or a time-delayed first or second bus access request signal, respectively, is disabled in the context of Claim 1.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 2. Accordingly, the Appellant respectfully requests that the final rejection of Claim 2 be withdrawn and that Claim 2 be passed to allowance.

G. CLAIM 3

Claim 3 recites the bus arbitrator of Claim 2, wherein the second delay of the delay circuit is greater than a maximum de-activation delay period associated with tri-state line drivers on a shared bus.

As Claim 3 depends from Claim 2, the arguments above with regard to Claim 2 apply here as well, and are incorporated herein by reference.

Furthermore, the Examiner's rejection makes an unfounded assertion: that the claimed maximum de-activation delay period associated with a tri-state line driver on a shared bus is equivalent to the switching time of an AND gate. The Examiner gives no explanation for choosing this particular equivalency, therefore the further assertion that the time for shifting an input through a shift register is inherently greater than the switching time of an AND gate does not address the purported obviousness of the claimed invention.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 3. Accordingly, the Appellant respectfully requests that the final rejection of Claim 3 be withdrawn and that Claim 3 be passed to allowance.

H. CLAIM 4

Claim 4 recites the bus arbitrator of Claim 3, wherein the comparator circuit includes a first AND gate with the first bus access request signal as a first input and the time-delayed first bus access request signal as a second input, and a second AND gate with the second bus access request signal as a first input and the time-delayed second bus access request signal as a second input.

As claim 4 depends from claim 3, the arguments above with regard to claim 3 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA* or *Marin* teaches a comparator circuit including first or second AND gates with first or second bus access request signals as a first input and time-delayed first or second bus access request signals as a second input, respectively, in the context of Claim 3.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 4. Accordingly, the Appellant respectfully requests that the final rejection of Claim 4 be withdrawn and that Claim 4 be passed to allowance.

I. CLAIM 9

Claim 9 recites a shared bus system, including:

> N bus devices capable of requesting access to a shared bus;
>
> M tristate line drivers, each of the M tristate line drivers having an input for receiving a logic bit from one of the N bus devices and an output for outputting the received logic bit to the shared bus, wherein each tristate line driver outputs the received logic bit when a line driver enable signal associated with the respective tristate line driver is enabled and an output of each tristate line driver is put into a high-impedance state when the associated line driver enable signal is disabled;
>
> a bus arbitrator operable to activate and de-activate the M tristate line drivers, the bus arbitrator comprising:
>
> an input circuit capable of receiving a first bus access request signal from a first of the N bus devices and a second bus access request signal from a second of the N bus devices, the input circuit also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled, the input circuit associated with a first delay;
>
> a delay circuit capable of receiving the first bus access request signal and generating therefrom a time-delayed first bus access request signal, the delay circuit also capable of receiving the second bus access request signal and generating therefrom a time-delayed second bus access request signal, the delay circuit associated with a second delay; and
>
> a comparator circuit capable of generating a first line driver enable signal only if both the first bus access request signal and the time-delayed first bus access request signal are enabled, the comparator circuit also capable of generating a second line driver enable signal only if both the second bus access request signal and the time-delayed second bus access request signal are enabled, wherein the second delay delays low-to-high transitions in the line driver enable signals by no more than one-half of a clock cycle of a clock signal,

> wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but does not delay high-to-low transitions in the first line driver enable signal.

The Examiner asserts that *AAPA* teaches a shared bus system having N bus devices that are capable of requesting access to a shared bus; M tristate line drivers, each with an input for receiving a logic bit from a bus device and an output for outputting the received logic bit to the shared bus, where each tristate line driver either outputs the logic bit to the shared bus or enters a high impedance state in response to an associated line driver enable signal. (*01/09/06 Office Action, Section 7, Page 5*). The Examiner further asserts that the *AAPA* describes a bus arbitrator including an input circuit receiving first and second bus access request signals from first and second bus devices, respectively, with the input circuit outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled. (*01/09/06 Office Action, Section 7, Page 5*). The Examiner also asserts that the AND gate and inverter of the *AAPA* inherently have a first delay and, because the first bus access request signal does not pass through the AND gate and inverter, high-to-low transitions in the first bus access request signal are not delayed by the first delay. (*01/09/06 Office Action, Section 7, Pages 5-6*).

The Examiner acknowledges that the *AAPA* does not teach a delay circuit generating time-delayed first and second bus access request signals, associated with a second delay, from the first and second bus access request signals, respectively, or a comparator circuit generating a first line driver enable signal only if both the first bus access request signal and the time-delayed first bus access request signal are enabled, and generates a second line driver enable signal only if both the second

bus access request signal and the time-delayed second bus access request signal are enabled, wherein the second delay delays low-to-high transitions in the first and second line driver enable signals by no more than one-half of a clock cycle of a clock signal. (*01/09/06 Office Action, Section 7, Page 6*). However, the Examiner asserts that *Marin* describes a delay circuit that receives a signal and generates a time-delayed version of the signal and a comparator circuit that generates an output signal only if both the signal and the time-delayed signal are enabled. (*01/09/06 Office Action, , Section 7, Page 6*). The Examiner further asserts that the delay circuit delays low-to-high transitions of the output signal by less than one-half of a clock cycle of a clock signal. (*01/09/06 Office Action, , Section 7, Page 6*). The Examiner also argues that, because the first delay of the *AAPA* is simply the propagation delay of a chain of two basic gates, the first delay is inherently shorter than that provided by the delay circuit of *Marin*, which is equal to the time for shifting an input through a shift register. (*01/09/06 Office Action, , Section 7, Pages 6-7*).

Finally, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of *AAPA* with the delay and comparator circuits of *Marin* on both the first and second bus access request signals "in order to provide a debounce delay period which ensures that the signal has reached a steady state and thus increases fault tolerance." (*01/09/06 Office Action, Section 7, Page 7*).

The rejection of claim 9 under 35 U.S.C. § 103 is improper and should be withdrawn for four reasons. First, the Examiner has made an unsupported assertion of a claim limitation being found inherently in the prior art. Second, the *Marin* reference, directed at debounce logic for keyswitches, is non-analogous art to Claim 9, directed to a shared bus system. Third, there is no motivation to

combine reference teachings. Fourth, no reasonable expectation of success in the combination of the references is found in the prior art.

1. The Examiner has made an unsupported assertion of a claim limitation being inherently taught in the prior art.

The Examiner asserts, without substantiation, that the delay of a signal propagating through an inverter and an AND gate is inherently shorter than that provided by the delay circuit of *Marin*. While the delay circuit of is labeled a shift register cell, the circuit functions as a simple latch or flip-flop, as acknowledged by the Examiner at Section 21, page 12, of the January 9, 2006 Office Action. The Appellant disagrees that the number of gates in a latch or flip-flop is such that the delay through the delay circuit of *Marin* is inherently greater than the delay of a signal propagating through an inverter and an AND gate. Furthermore, there is no teaching in *Marin* of the implementation of its delay circuit to inform the Examiner's assertion that its propagation delay is necessarily greater than that through an inverter and an AND gate.

2. The Marin reference is non-analogous art to the claims of the present application.

The *Marin* reference is directed to debounce logic in a keyboard switch scanner. When a keyswitch is depressed, the contacts may bounce. The *Marin* reference teaches that it is advisable for a switch scanner to combine three successive samples of the keyswitch status to ensure that the contacts have ceased bouncing. (*Marin, Col. 7, lines 50-56*) In contrast, the Claim 9 is directed to a shared bus system that includes bus devices coupled to the shared bus by tristate line drivers under

the control of a bus arbitrator. The claimed bus arbitrator eliminates bus contentions by ensuring that the turn-off time of a line driver ceasing to drive the shared bus is shorter than the turn-on time of a line driver beginning to drive the shared bus. *(Application, page 6, first paragraph)*. As such, the *Marin* reference, directed at sensing mechanical switch contact bounce, is not analogous art to the arbitrator for a shared bus system claimed in the present application.

3. There is no motivation to combine the cited references as proposed by the Examiner.

There is no motivation to combine the cited references as proposed by the Examiner. The Examiner's proposed motivation for adding elements of the circuit of *Marin* to the bus arbitrator of the *AAPA* does not address any problem faced by the person of ordinary skill designing a bus arbitrator. A bus access request signal is an output of a semiconductor switch, not a mechanical switch, and, as such, is not subject to contact bounce. Thus, the person of ordinary skill designing a bus arbitrator would have no motivation to "provide a debounce delay period which ensures that the signal has reached a steady state and thus increases fault tolerance" as suggested by the examiner.

Furthermore, the *Marin* reference describes the use of two shift register cells and a three-input AND gate, to combine a current sample of keyswitch contact status with two preceding samples. The circuit signals a switch closure only when three successive samples indicate that the switch is closed. The Examiner asserts, however, that a person of ordinary skill would have found it obvious to modify the bus arbitrator of the prior art with a subset of the circuitry of the *Marin* reference—only a single shift register cell and a two-input AND gate. The Appellant respectfully submits that the Examiner improperly uses the claims of the present application as a template in

selecting portions of the *Marin* reference to combine with the prior art bus arbitrator. Thus, there is no motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine reference teachings as proposed in the Office Action.

4. No reasonable expectation of success in the combination of the references is found in the prior art.

Finally, even were a person of ordinary skill to combine portions of the circuitry of the *Marin* reference with the prior art bus arbitrator, as proposed by the Examiner, no reasonable expectation of success in such a combination may be found in the prior art. While *Marin* describes the benefit of using two shift register cells and a three-input AND gate, it teaches no benefit in using a single shift register cell and a two-input AND gate. As such, the expectation of success in the combination of cited references is found not in the prior art, but in the Applicant's disclosure.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 9. Accordingly, the Appellant respectfully requests that the final rejection of Claim 9 be withdrawn and that Claim 9 be passed to allowance.

J. CLAIM 10

Claim 10 recites the shared bus system of Claim 9, wherein the comparator circuit disables the first line driver enable signal if either of the first bus access request signal or the time-delayed

first bus access request signal is disabled, and disables the second line driver enable signal if either of the second bus access request signal or the time-delayed second bus access request signal is disabled.

As claim 10 depends from claim 9, the arguments above with regard to claim 9 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA* or *Marin* teaches a comparator circuit disabling a first or second line driver enable signal if either of a first or second bus access request signal or a time-delayed first or second bus access request signal, respectively, is disabled in the context of Claim 9.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 10. Accordingly, the Appellant respectfully requests that the final rejection of Claim 10 be withdrawn and that Claim 10 be passed to allowance.

K. CLAIM 11

Claim 11 recites the shared bus system of Claim 10, wherein the second delay of the delay circuit is greater than a maximum de-activation delay period associated with tri-state line drivers on a shared bus.

As Claim 11 depends from Claim 10, the arguments above with regard to Claim 10 apply here as well, and are incorporated herein by reference.

Furthermore, the Examiner's rejection makes an unfounded assertion: that the claimed maximum de-activation delay period associated with a tri-state line driver on a shared bus is equivalent to the switching time of an AND gate. The Examiner gives no explanation for choosing

this particular equivalency, therefore the further assertion that the time for shifting an input through a shift register is inherently greater than the switching time of an AND gate does not address the purported obviousness of the claimed invention.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 11. Accordingly, the Appellant respectfully requests that the final rejection of Claim 11 be withdrawn and that Claim 11 be passed to allowance.

L. CLAIM 12

Claim 12 recites the bus arbitrator of Claim 11, wherein the comparator circuit includes a first AND gate with the first bus access request signal as a first input and the time-delayed first bus access request signal as a second input, and a second AND gate with the second bus access request signal as a first input and the time-delayed second bus access request signal as a second input.

As claim 12 depends from claim 11, the arguments above with regard to claim 11 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA* or *Marin* teaches a comparator circuit including first or second AND gates with first or second bus access request signals as a first input and time-delayed first or second bus access request signals as a second input, respectively, in the context of Claim 11.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 12. Accordingly, the

Appellant respectfully requests that the final rejection of Claim 12 be withdrawn and that Claim 12 be passed to allowance.

M. CLAIM 17

Claim 17 recites a method for use in a shared bus system comprising N bus devices capable of requesting access to a shared bus. The method is for activating and de-activating a plurality of tristate line drivers coupled between the shared bus and the N bus devices, and includes the steps of:

> receiving a first bus access request signal from a first of the bus devices;
> receiving a second bus access request signal from a second of the bus devices;
> blocking the second bus access request signal when the first bus access request signal is enabled, the blocking step associated with a first delay;
> generating from the first bus access request signal a time-delayed first bus access request signal and generating from the second bus access request signal a time-delayed second bus access request signal, the generating step associated with a second delay;
> comparing the first bus access request signal and the time-delayed first bus access request signal and generating a first line driver enable signal only if both of the first bus access request signal and the time-delayed first bus access request signal are enabled; and
> comparing the second bus access request signal and the time-delayed second bus access request signal and generating a second line driver enable signal only if both of the second bus access request signal and the time-delayed second bus access request signal are enabled,
> wherein the second delay delays low-to-high transitions in the line driver enable signals by no more than one-half of a clock cycle of a clock signal, and
> wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but does not delay high-to-low transitions in the first line driver enable signal.

The Examiner asserts that Claim 17 recites limitations that are substantially equivalent to those of Claim 9 and rejects Claim 17 under similar reasoning as applied to Claim 9.

The rejection of claim 17 under 35 U.S.C. § 103 is improper and should be withdrawn for four reasons. First, the Examiner has made an unsupported assertion of a claim limitation being found inherently in the prior art. Second, the *Marin* reference, directed at debounce logic for keyswitches, is non-analogous art to Claim 17, directed to a method of activating a plurality of tri-state line drivers in a shared bus system. Third, there is no motivation to combine reference teachings. Fourth, no reasonable expectation of success in the combination of the references is found in the prior art.

1. The Examiner has made an unsupported assertion of a claim limitation being inherently taught in the prior art.

The Examiner asserts, without substantiation, that the delay of a signal propagating through an inverter and an AND gate is inherently shorter than that provided by the delay circuit of *Marin*. While the delay circuit of is labeled a shift register cell, the circuit functions as a simple latch or flip-flop. The Appellant disagrees that the number of gates in a latch or flip-flop is such that the delay through the delay circuit of *Marin* is, without more, inherently greater than the delay of a signal propagating through an inverter and an AND gate. Furthermore, there is no teaching in *Marin* of the implementation of its delay circuit to inform the Examiner's assertion that its propagation delay is necessarily greater than that through an inverter and an AND gate.

2. The Marin reference is non-analogous art to the claims of the present application.

The *Marin* reference is directed to debounce logic in a keyboard switch scanner. When a keyswitch is depressed, the contacts may bounce. The *Marin* reference teaches that it is advisable for a switch scanner to combine three successive samples of the keyswitch status to ensure that the contacts have ceased bouncing. (*Marin, Col. 7, lines 50-56*) In contrast, the claims of the present application are directed to a method of activating a plurality of tri-state line drivers in a shared bus system. The claimed invention eliminates bus contentions by ensuring that the turn-off time of a line driver ceasing to drive the shared bus is shorter than the turn-on time of a line driver beginning to drive the shared bus. *(Application, page 6, first paragraph)*. As such, the *Marin* reference, directed at sensing mechanical switch contact bounce, is not analogous art to the arbitrator for a shared bus system claimed in the present application.

3. There is no motivation to combine the cited references as proposed by the Examiner.

There is no motivation to combine the cited references as proposed by the Examiner. The Examiner's proposed motivation for adding elements of the circuit of *Marin* to the bus arbitrator of the *AAPA* does not address any problem faced by the person of ordinary skill designing a bus arbitrator. A bus access request signal is an output of a semiconductor switch, not a mechanical switch, and, as such, is not subject to contact bounce. Thus, the person of ordinary skill designing a bus arbitrator would have no motivation to "provide a debounce delay period which ensures that the signal has reached a steady state and thus increases fault tolerance" as suggested by the examiner.

Furthermore, the *Marin* reference describes the use of two shift register cells and a three-input AND gate, to combine a current sample of keyswitch contact status with two preceding samples. The circuit signals a switch closure only when three successive samples indicate that the switch is closed. The Examiner asserts, however, that a person of ordinary skill would have found it obvious to modify the bus arbitrator of the prior art with a subset of the circuitry of the *Marin* reference—only a single shift register cell and a two-input AND gate. The Appellant respectfully submits that the Examiner improperly uses the claims of the present application as a template in selecting portions of the *Marin* reference to combine with the prior art bus arbitrator. Thus, there is no motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine reference teachings as proposed in the Office Action.

4. No reasonable expectation of success in the combination of the references is found in the prior art.

Finally, even were a person of ordinary skill to combine portions of the circuitry of the *Marin* reference with the prior art bus arbitrator, as proposed by the Examiner, no reasonable expectation of success in such a combination may be found in the prior art. While *Marin* describes the benefit of using two shift register cells and a three-input AND gate, it teaches no benefit in using a single shift register cell and a two-input AND gate. As such, the expectation of success in the combination of cited references is found not in the prior art, but in the Applicant's disclosure.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 17. Accordingly, the

Appellant respectfully requests that the final rejection of Claim 17 be withdrawn and that Claim 17 be passed to allowance.

N. CLAIM 18

Claim 18 recites the method of Claim 17, including the further steps of disabling the first line driver enable signal if either of the first bus access request signal or the time-delayed first bus access request signal is disabled, and disabling the second line driver enable signal if either of the second bus access request signal or the time-delayed second bus access request signal is disabled.

As claim 18 depends from claim 17, the arguments above with regard to claim 17 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA* or *Marin* teaches disabling a first or second line driver enable signal if either of a first or second bus access request signal or a time-delayed first or second bus access request signal, respectively, is disabled in the context of Claim 17.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 18. Accordingly, the Appellant respectfully requests that the final rejection of Claim 18 be withdrawn and that Claim 18 be passed to allowance.

O. CLAIM 19

Claim 19 recites the method of Claim 18, wherein the second delay of the delay circuit is greater than a maximum de-activation delay period associated with tri-state line drivers on a shared bus.

As Claim 19 depends from Claim 18, the arguments above with regard to Claim 18 apply here as well, and are incorporated herein by reference.

Furthermore, the Examiner's rejection makes an unfounded assertion: that the claimed maximum de-activation delay period associated with a tri-state line driver on a shared bus is equivalent to the switching time of an AND gate. The Examiner gives no explanation for choosing this particular equivalency, therefore the further assertion that the time for shifting an input through a shift register is inherently greater than the switching time of an AND gate does not address the purported obviousness of the claimed invention.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 19. Accordingly, the Appellant respectfully requests that the final rejection of Claim 19 be withdrawn and that Claim 19 be passed to allowance.

P. CLAIM 20

Claim 20 recites the method of Claim 19, wherein the comparing steps use a comparator circuit that includes a first AND gate with the first bus access request signal as a first input and the time-delayed first bus access request signal as a second input, and a second AND gate with the

second bus access request signal as a first input and the time-delayed second bus access request signal as a second input.

As claim 20 depends from claim 19, the arguments above with regard to claim 19 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA* or *Marin* teaches a comparator circuit including first or second AND gates with first or second bus access request signals as a first input and time-delayed first or second bus access request signals as a second input, respectively, in the context of Claim 19.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 20. Accordingly, the Appellant respectfully requests that the final rejection of Claim 20 be withdrawn and that Claim 20 be passed to allowance.

Q. CLAIM 21

Claim 2 recites the bus arbitrator of Claim 1, wherein the input circuit includes an inverter capable of receiving and inverting the first bus access request signal, and an AND gate capable of receiving the inverted first bus access request signal and the second bus access request signal, the AND gate also capable of outputting or blocking the second bus access request signal when the first bus access request signal is not enabled or enabled, respectively.

As claim 21 depends from claim 1, the arguments above with regard to claim 1 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA* or *Marin* teaches an input circuit including an inverter capable of receiving and inverting the first bus access request signal, and an AND gate capable of receiving the inverted first bus access request signal and the second bus access request signal, the AND gate also capable of outputting or blocking the second bus access request signal when the first bus access request signal is not enabled or enabled, respectively, in the context of Claim 1.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 21. Accordingly, the Appellant respectfully requests that the final rejection of Claim 21 be withdrawn and that Claim 21 be passed to allowance.

II. GROUND OF REJECTION #2

The rejection of Claims 5-6 and 13-14 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

A. OVERVIEW

Claims 5-6 and 13-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *AAPA* in view of *Marin* and further in view of U.S. Patent No. 5,306,963 to *Leak*, et al. ("*Leak*").

B. THE *LEAK* REFERENCE

Leak describes a noise filter to eliminate short, multiple pulses output from an address transition detection circuit. (*Abstract*). The noise filter includes a transition pulse generation circuit

that generates a pulse of a predetermined length upon any change in value of a binary input signal. The transition pulse generation circuit operates by performing an exclusive-or operation on the input signal and a delayed version of the signal after passage through an even number of inverters. (*Col. 3, Line 64, through Col. 4, Line 55*).

C. CLAIM 5

Claim 5 recites the bus arbitrator of Claim 3, wherein the delay circuit is an asynchronous delay circuit.

As claim 5 depends from claim 3, the arguments above with regard to claim 3 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA*, *Marin* or *Leak* teaches an asynchronous delay circuit in the context of Claim 3.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin-Leak* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 5. Accordingly, the Appellant respectfully requests that the final rejection of Claim 5 be withdrawn and that Claim 5 be passed to allowance.

D. CLAIM 6

Claim 6 recites the bus arbitrator of Claim 5, wherein the delay circuit includes first and second sets of an even number of inverters connected in series, wherein a first inverter in each of the first and second sets receives the first and second bus access request signals, respectively, and a last

inverter in each of the first and second sets generates the time-delayed first and second bus access request signals, respectively.

As claim 6 depends from claim 5, the arguments above with regard to claim 5 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA*, *Marin* or *Leak* teaches a delay circuit including first and second sets of an even number of inverters connected in series, wherein a first inverter in each of the first and second sets receives first and second bus access request signals, respectively, and a last inverter in each of the first and second sets generates time-delayed first and second bus access request signals, respectively, in the context of Claim 5.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin-Leak* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 6. Accordingly, the Appellant respectfully requests that the final rejection of Claim 6 be withdrawn and that Claim 6 be passed to allowance.

E. CLAIM 13

Claim 13 recites the shared bus system of Claim 11, wherein the delay circuit is an asynchronous delay circuit.

As claim 13 depends from claim 11, the arguments above with regard to claim 11 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA*, *Marin* or *Leak* teaches an asynchronous delay circuit in the context of Claim 11.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin-Leak* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 13. Accordingly, the Appellant respectfully requests that the final rejection of Claim 13 be withdrawn and that Claim 13 be passed to allowance.

F. CLAIM 14

Claim 14 recites the shared bus system of Claim 13, wherein the delay circuit includes first and second sets of an even number of inverters connected in series, wherein a first inverter in each of the first and second sets receives the first and second bus access request signals, respectively, and a last inverter in each of the first and second sets generates the time-delayed first and second bus access request signals, respectively.

As claim 14 depends from claim 13, the arguments above with regard to claim 13 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA*, *Marin* or *Leak* teaches a delay circuit including first and second sets of an even number of inverters connected in series, wherein a first inverter in each of the first and second sets receives first and second bus access request signals, respectively, and a last inverter in each of the first and second sets generates time-delayed first and second bus access request signals, respectively, in the context of Claim 13.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin-Leak* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 14.

Accordingly, the Appellant respectfully requests that the final rejection of Claim 14 be withdrawn and that Claim 14 be passed to allowance.

III. GROUND OF REJECTION #3

The rejection of Claims 7-8 and 15-16 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

A. OVERVIEW

Claims 7-8 and 15-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over *AAPA* in view of *Marin* and further in view of FREDERICK J. HILL & GERALD R. PETERSON, COMPUTER AIDED LOGICAL DESIGN: WITH EMPHASIS ON VLSI § 4.1 (4th ed. 1993) ("*Hill*").

B. THE *HILL* REFERENCE

Hill describes the implementation of binary logic elements in metal oxide semiconductor (MOS) integrated circuits. In some MOS integrated circuits, an AND gate may be implemented as a NAND gate whose output passes through an inverter.

C. CLAIM 7

Claim 7 recites the bus arbitrator of Claim 3, wherein the delay circuit is a synchronous delay circuit.

As claim 7 depends from claim 3, the arguments above with regard to claim 3 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA*, *Marin* or *Hill* teaches a synchronous delay circuit in the context of Claim 3.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin-Hill* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 7. Accordingly, the Appellant respectfully requests that the final rejection of Claim 7 be withdrawn and that Claim 7 be passed to allowance.

D. CLAIM 8

Claim 8 recites the bus arbitrator of Claim 7, wherein the delay circuit includes first and second flip-flops, each having an input receiving the first and second bus access request signals, respectively, and each having an output coupled to the comparator circuit that generates said time-delayed first and second bus access request signals, respectively. The delay circuit also includes first and second inverters, each having an input receiving the clock signal and each having an output coupled to a clock input of the first and second flip-flops, respectively.

As claim 8 depends from claim 7, the arguments above with regard to claim 7 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA*, *Marin* or *Hill* teaches a delay circuit including first and second flip-flops, each having an input receiving the first and second bus access request signals, respectively, and each having an output coupled to the comparator circuit that generates said time-

delayed first and second bus access request signals, respectively, and further including first and second inverters, each having an input receiving the clock signal and each having an output coupled to a clock input of the first and second flip-flops, respectively, in the context of Claim 7.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin-Hill* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 8. Accordingly, the Appellant respectfully requests that the final rejection of Claim 8 be withdrawn and that Claim 8 be passed to allowance.

E. CLAIM 15

Claim 15 recites the shared bus system of Claim 11, wherein the delay circuit is a synchronous delay circuit.

As claim 15 depends from claim 11, the arguments above with regard to claim 11 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA*, *Marin* or *Hill* teaches a synchronous delay circuit in the context of Claim 11.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin-Hill* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 15. Accordingly, the Appellant respectfully requests that the final rejection of Claim 15 be withdrawn and that Claim 15 be passed to allowance.

F. CLAIM 16

Claim 16 recites the shared bus system of Claim 15, wherein the delay circuit includes first and second flip-flops, each having an input receiving the first and second bus access request signals, respectively, and each having an output coupled to the comparator circuit that generates said time-delayed first and second bus access request signals, respectively. The delay circuit also includes first and second inverters, each having an input receiving the clock signal and each having an output coupled to a clock input of the first and second flip-flops, respectively.

As claim 16 depends from claim 15, the arguments above with regard to claim 15 apply here as well, and are incorporated herein by reference.

Furthermore, nothing in the *AAPA*, *Marin* or *Hill* teaches a delay circuit including first and second flip-flops, each having an input receiving the first and second bus access request signals, respectively, and each having an output coupled to the comparator circuit that generates said time-delayed first and second bus access request signals, respectively, and further including first and second inverters, each having an input receiving the clock signal and each having an output coupled to a clock input of the first and second flip-flops, respectively, in the context of Claim 15.

For these reasons, the Examiner fails to establish that the proposed *AAPA-Marin-Hill* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 16. Accordingly, the Appellant respectfully requests that the final rejection of Claim 16 be withdrawn and that Claim 16 be passed to allowance.

SUMMARY

The Appellant has demonstrated that the present invention as claimed is clearly distinguishable over the prior art cited of record. Therefore, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the final rejection of the Examiner and instruct the Examiner to issue a notice of allowance of all claims.

The Appellant paid the appropriate fee to cover the cost of the APPEAL BRIEF filed July 17, 2006. The Appellant does not believe that any additional fees are due. However, the Commissioner is hereby authorized to charge any additional fees (including any extension of time fees) or credit any overpayments to Munck Butrus Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS, P.C.

Date: Aug 24, 2006

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APPENDIX A

PENDING CLAIMS APPENDIX

1. A bus arbitrator comprising:

an input circuit receiving a first bus access request signal from a first bus device and a second bus access request signal from a second bus device, the input circuit outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled, the input circuit associated with a first delay;

a delay circuit generating a time-delayed first bus access request signal from the first bus access request signal and a time-delayed second bus access request signal from the second bus access request signal, the delay circuit associated with a second delay; and

a comparator circuit generating a first line driver enable signal only if both the first bus access request signal and the time-delayed first bus access request signal are enabled and generating a second line driver enable signal only if both the second bus access request signal and the time-delayed second bus access request signal are enabled,

wherein the second delay delays low-to-high transitions in the first and second line driver enable signals by no more than one-half of a clock cycle of a clock signal, and wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but does not delay high-to-low transitions in the first line driver enable signal.

2. The bus arbitrator as set forth in claim 1 wherein the comparator circuit:

disables the first line driver enable signal if either of the first bus access request signal or the time-delayed first bus access request signal is disabled; and

disables the second line driver enable signal if either of the second bus access request signal or the time-delayed second bus access request signal is disabled.

3. The bus arbitrator as set forth in claim 2 wherein the second delay of the delay circuit is greater than a maximum de-activation delay period associated with tri-state line drivers on a shared bus.

4. The bus arbitrator as set forth in claim 3 wherein the comparator circuit comprises:

a first AND gate having a first input receiving the first bus access request signal and a second input receiving the time-delayed first bus access request signal; and

a second AND gate having a first input receiving the second bus access request signal and a second input receiving the time-delayed second bus access request signal.

5. The bus arbitrator as set forth in claim 3 wherein the delay circuit is an asynchronous delay circuit.

6. The bus arbitrator as set forth in claim 5 wherein the delay circuit comprises:

a first set of an even number of inverters connected in series, wherein a first inverter in the first set receives the first bus access request signal and a last inverter in the first set generates the time-delayed first bus access request signal; and

a second set of an even number of inverters connected in series, wherein a first inverter in the second set receives the second bus access request signal and a last inverter in the second set generates the time-delayed second bus access request signal.

7. The bus arbitrator as set forth in claim 3 wherein the delay circuit is a synchronous delay circuit.

8. The bus arbitrator as set forth in claim 7 wherein the delay circuit comprises:

a first flip-flop having an input receiving the first bus access request signal and an output coupled to the comparator circuit that generates said time-delayed first bus access request signal;

a first inverter having an input receiving the clock signal and an output coupled to a clock input of the first flip-flop;

a second flip-flop having an input receiving the second bus access request signal and an output coupled to the comparator circuit that generates the time-delayed second bus access request signal; and

a second inverter having an input receiving the clock signal and an output coupled to a clock input of the second flip-flop.

9. A shared bus system comprising:

N bus devices capable of requesting access to a shared bus;

M tristate line drivers, each of the M tristate line drivers having an input for receiving a logic bit from one of the N bus devices and an output for outputting the received logic bit to the shared bus, wherein each tristate line driver outputs the received logic bit when a line driver enable signal associated with the respective tristate line driver is enabled and an output of each tristate line driver is put into a high-impedance state when the associated line driver enable signal is disabled;

a bus arbitrator operable to activate and de-activate the M tristate line drivers, the bus arbitrator comprising:

an input circuit capable of receiving a first bus access request signal from a first of the N bus devices and a second bus access request signal from a second of the N bus devices, the input circuit also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled, the input circuit associated with a first delay;

a delay circuit capable of receiving the first bus access request signal and generating therefrom a time-delayed first bus access request signal, the delay circuit also capable of receiving the second bus access request signal and generating therefrom a time-delayed second bus access request signal, the delay circuit associated with a second delay; and

a comparator circuit capable of generating a first line driver enable signal only if both the first bus access request signal and the time-delayed first bus access request signal are enabled, the comparator circuit also capable of generating a second line driver enable signal only if both the second bus access request signal and the time-delayed second bus access request signal are enabled, wherein the second delay delays low-to-high transitions in the line driver enable signals by no more than one-half of a clock cycle of a clock signal,

wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but does not delay high-to-low transitions in the first line driver enable signal.

10. The shared bus system as set forth in claim 9 wherein the comparator circuit:

disables the first line driver enable signal if either the first bus access request signal or the time-delayed first bus access request signal is disabled; and

disables the second line driver enable signal if either of the second bus access request signal or the time-delayed second bus access request signal is disabled.

11. The shared bus system as set forth in claim 10 wherein the second delay of the delay circuit is greater than a maximum de-activation delay period associated with the tri-state line drivers.

12. The shared bus system as set forth in claim 11 wherein the comparator circuit comprises:

a first AND gate having a first input for receiving the first bus access request signal and a second input for receiving the time-delayed first bus access request signal; and

a second AND gate having a first input for receiving the second bus access request signal and a second input for receiving the time-delayed second bus access request signal.

13. The shared bus system as set forth in claim 11 wherein the delay circuit is an asynchronous delay circuit.

14. The shared bus system as set forth in claim 13 wherein the delay circuit comprises:

a first set of an even number of inverters connected in series, wherein a first inverter in the first set receives the first bus access request signal and a last inverter in the first set generates the time-delayed first bus access request signal; and

a second set of an even number of inverters connected in series, wherein a first inverter in the second set receives the second bus access request signal and a last inverter in the second set generates the time-delayed second bus access request signal.

15. The shared bus system as set forth in claim 11 wherein the delay circuit is a synchronous delay circuit.

16. The shared bus system as set forth in claim 15 wherein the delay circuit comprises:

a first flip-flop having an input capable of receiving the first bus access request signal and an output coupled to the comparator circuit that generates the time-delayed first bus access request signal;

a first inverter having an input capable of receiving the clock signal and an output coupled to a clock input of the first flip-flop;

a second flip-flop having an input capable of receiving the second bus access request signal and an output coupled to the comparator circuit that generates the time-delayed second bus access request signal; and

a second inverter having an input capable of receiving the clock signal and an output coupled to a clock input of the second flip-flop.

17. For use in a shared bus system comprising N bus devices capable of requesting access to a shared bus, a method for activating and de-activating a plurality of tristate line drivers coupled between the shared bus and the N bus devices, the method comprising the steps of:

receiving a first bus access request signal from a first of the bus devices;

receiving a second bus access request signal from a second of the bus devices;

blocking the second bus access request signal when the first bus access request signal is enabled, the blocking step associated with a first delay;

generating from the first bus access request signal a time-delayed first bus access request signal and generating from the second bus access request signal a time-delayed second bus access request signal, the generating step associated with a second delay;

comparing the first bus access request signal and the time-delayed first bus access request signal and generating a first line driver enable signal only if both of the first bus access request signal and the time-delayed first bus access request signal are enabled; and

comparing the second bus access request signal and the time-delayed second bus access request signal and generating a second line driver enable signal only if both of the second bus access request signal and the time-delayed second bus access request signal are enabled,

wherein the second delay delays low-to-high transitions in the line driver enable signals by no more than one-half of a clock cycle of a clock signal, and

wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but does not delay high-to-low transitions in the first line driver enable signal.

18. The method as set forth in claim 17 further comprising the steps of:

disabling the first line driver enable signal if either of the first bus access request signal and the time-delayed first bus access request signal is disabled; and

disabling the second line driver enable signal if either of the second bus access request signal and the time-delayed second bus access request signal is disabled.

19. The method as set forth in claim 18 wherein the second delay is greater than a maximum de-activation delay period associated with the plurality of tri-state line drivers.

20. The method as set forth in claim 19 wherein the comparing steps comprise using a comparator circuit, the comparator circuit comprising:

a first AND gate having a first input for receiving the first bus access request signal and a second input for receiving the time-delayed first bus access request signal; and

a second AND gate having a first input for receiving the second bus access request signal and a second input for receiving the time-delayed second bus access request signal.

21. The bus arbitrator of Claim 1, wherein the input circuit comprises:

an inverter capable of receiving and inverting the first bus access request signal; and

an AND gate capable of receiving the inverted first bus access request signal and the second bus access request signal, the AND gate also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled.

APPENDIX B

EVIDENCE APPENDIX

None

APPENDIX C

RELATED PROCEEDINGS APPENDIX

None